

Nano power VFC Includes Self-Compensating Charge Pump

Of the many starting points for voltage-to-frequency converter (VFC) design, one of the golden oldies is the classic diode-capacitor charge pump. An example of this fundamental circuit is represented by D1, D2, C1, and C2 (see the figure). Analysis of this simple topology reveals that each cycle of A1's 4-V p-p square wave output will inject a charge onto C5 given by :

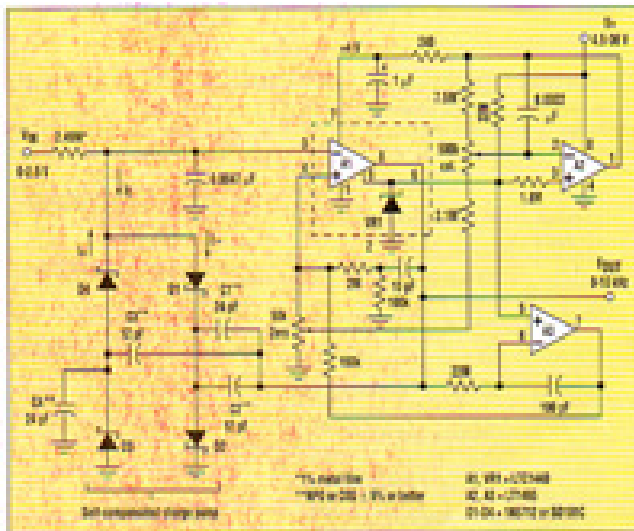
$$Q^- = -(C1 + C2 + C_s)[(C1 + C2) / (C1 + C2 + C_s) - 2V_d]$$

Where :

V = the peak-to-peak pump-drive voltage generated by A1

C_s = stray capacitance at the Dn/Cn common node including diode junction capacitance

V_d = diode forward voltage drop



An obvious snag with this scheme is that the need to cope with temperature dependence of V_d (approximately - 2 mV/°C) inevitably complicates VFCs that use this basic pump. Elegant compensation circuits exist that work by tweaking V so as to cancel out V_d (pioneered by Bob Pease; and for an interesting twist by Jim Williams, see Linear Technology's LT1495 data sheet) through relationships like : V = V_{REF} + 2 V_d. But these methods sometimes run into trouble, particularly in micro power applications where the need to make Q dinky (thereby minimizing current

consumption) runs afoul of V_s >> 0.

The figure illustrates a different V_d fix. In this circuit, D3, D4, C3, and C4 work together to make a compensatory charge pulse for each A1 output cycle :

$$Q^+ = (C3 + C4 + C_s)[(V * C3) / (C3 + C4 + C_s) - 2V_d]$$

The pay off is that, if we assume C1 = C4 and C2 = C3, and equality of V_ds and C_ss, then each full cycle of A1 will inject onto C5 a net charge pulse of :

$$(Q^+) + (Q^-) = (C1 + C2 + C_s)\{V[(C2 - (C1 + C2))/(C1 + C2 + C_s) + 2V_d - 2V_d]\} \\ = V[C2 - (C1 + C2)] = -V * C1$$

Not only do we get compensation for the bothersome V_{ds} , but the effects of stray capacitance also get rubbed out.

The rest of the figure uses the new self-compensating pump to close a feedback loop around A1 so that input currents are balanced by : $I_f = -F_0 * V * C1 = 0$ to $-1\mu A$ as V_{in} Goes from 0 to +2.5 V and F_0 goes from 0 to 10 kHz. A2 serves to develop a stable drive source V from THE ltc1440 1.2-V internal reference and will do so for supply voltages from 4.5 to 36 V. A3 is a startup circuit that restores oscillation of the A1 charge pump, ac-coupled feedback loop if lockup occurs from, say, input over range.

Overall temperature coefficient of the converter depends on matching of all pump capacitances, including circuit board layout contribution to C_s parasitics. Just $\pm 5\%$ tolerance is good enough to reduce the charge-pump temperature coefficient to approximately 50 ppm/ $^{\circ}C$. Converter linearity is $\pm 0.03\%$ and current draw is an unexcelled 6.5 to 9 μA @ $V_+ = 5V$ as F_0 goes from 0 to 10kHz.